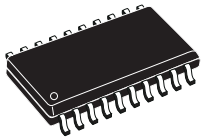
L9380

Triple high-side MOSFET driver

Features

- Overvoltage charge pump shut off
- For V_S > 25 V
- Reverse battery protection (referring to the application circuit diagram)
- Programmable overload protection function for channel 1 and 2
- Open ground protection function for channel 1 and 2
- Constant gate charge/discharge current



SO20

Description

The L9380 device is a controller for three external N-channel power MOS transistors in "High-Side Switch" configuration.

It is intended for relays replacement in automotive electric control units.

Table 1. Device summary

Order code	Package	Packing
L9380	SO20	Tube
L9380-TR	SO20	Tape and reel

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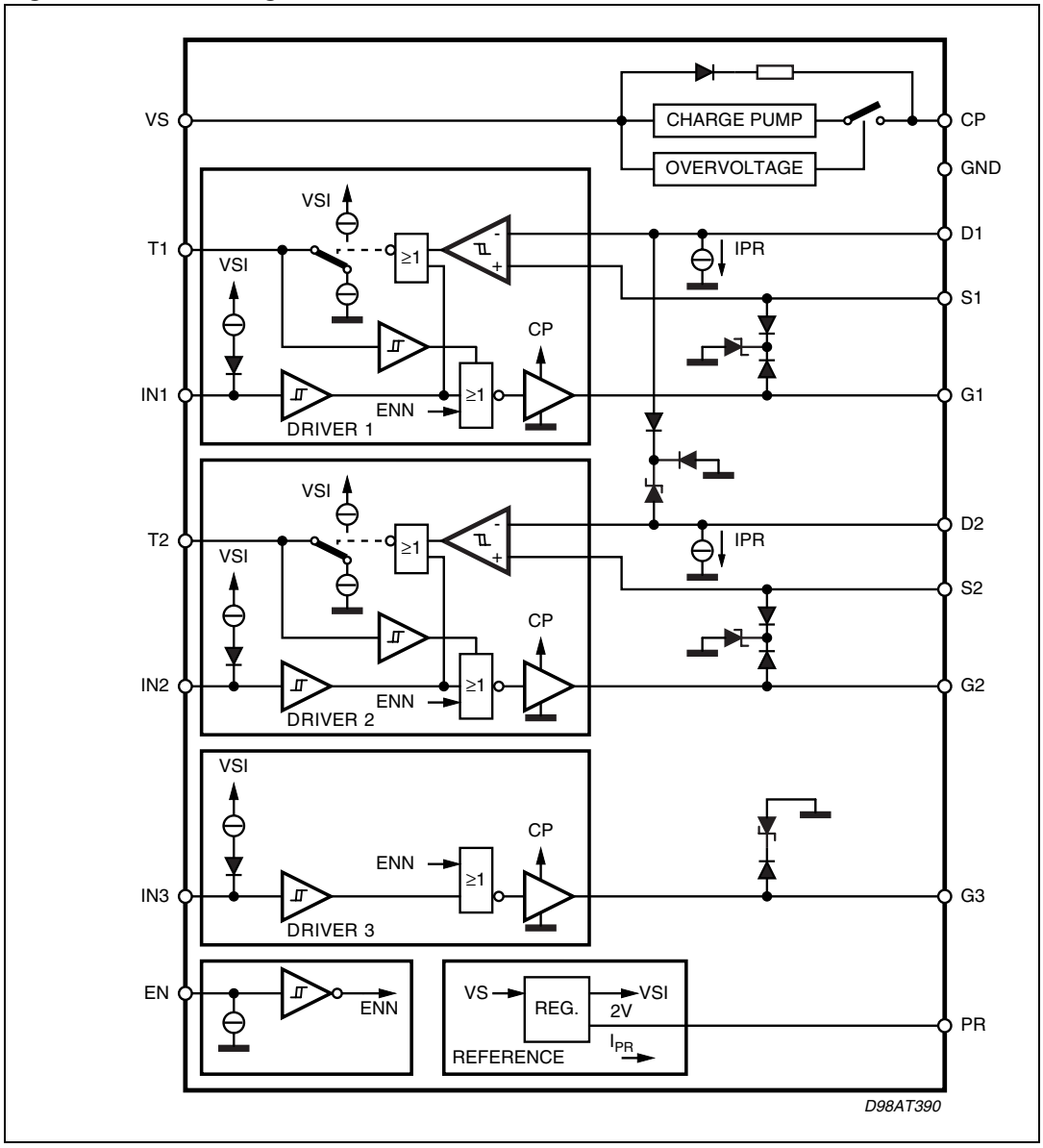
1 Block diagram

Figure 1. Block diagram



2 Pins description

Figure 2. Pins connection (top view)

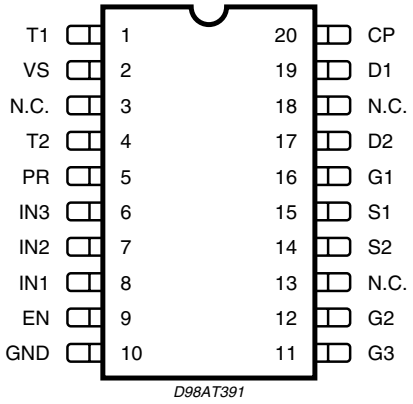


Table 2. Pins function

N°	Pin name	Function
1	T1	Timer capacitor; the capacitor defines the time for the channel 1 shut down, after overload of the external MOS transistor has been detected.
2	V_S	Supply voltage.
4	T2	Timer capacitor; the capacitor defines the time for the channel 2 shut down, after overload of the external MOS transistor has been detected.
5	PR	Programming resistor for overload detetcion threshold; the resistor from this pin to ground defines the drain pin current and the charging of the timer capacitor.
6	IN3	Input 3; equal to IN1.
7	IN2	Input 2; equal to IN1.
8	IN1	Input 1; logic signal applied to this pin controls the driver 1; this pin features a current source to assure defined high status when the pin is open.
9	EN	Enable logic signal high on this pin enables all channels
10	GND	Ground
11	G3	Gate 3 driver output; current source from CP or ground
12	G2	Gate 2 driver output; current source from CP or ground
14	S2	Source 2 sense input; monitors the source voltage.
15	S1	Source 1 sense input; monitors the source voltage.
16	G1	Gate 1 driver output; current source from CP or ground
17	D2	Drain 2 sense input; a programmable input bias current defines the drop across the external resistor R_{D1}; this drop fixes the overload threshold of the external MOS.
19	D1	Drain 1 sense input; a programmable input bias current defines the drop across the external resistor R_{D1}; this drop fixes the overload threshold of the external MOS.
20	CP	Charge pump capacitor; a alternating current source at this pin charges the connected capacitor C_{CP} to a voltage 10V higher than V_S; the charge stored in this capacitor is than used to charge all the three gates of the power MOS transistors.
3, 13, 18	NC	Not connected

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	DC supply voltage	-0.3 to +27	V
V_S	Supply voltage pulse (t ≤ 400 ms)	45	V
$\Delta V_S/dt$	Supply voltage slope	-10 to +10	V/µs
$V_{IN,EN}$	Input / enable voltage	-0.3 to +7	V
V_T	Timer voltage	-0.3 to 27	V
$V_{D, G, S}$	Drain, gate, source voltage	-15 to +27	V
$V_{D, G, S}$	Drain, gate, source voltage pulse (t ≤ 400 ms)	45	V
$I_{D, G, S}$	Drain, gate, source current (t ≤ 2 ms)	0 to +4	mA
T_j	Operating junction temperature	-40 to 150	°C
T_{stg}	Storage temperature	-65 to 150	°C

Note: ESD for all pins, except the timer pins, are according to MIL 883C, tested at 2 kV, corresponds to a maximum energy dissipation of 0.2 mJ.
The timer pins are tested with 800 V.

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance junction to ambient	100	°C/W

3.3 Electrical characteristics

Table 5. Electrical characteristics
(7 V ≤ V_S ≤ 18.5 V; -40° C ≤ T_J ≤ 150 °C, unless otherwise specified.)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply						
I_{VS}	Static operating supply current	V_S = 14 V			2.5	mA
Charge pump						
V_{CP}	Charge pump voltage above V_S		8		17	V
I_{CP}	Charge pump current	V_S = 7 V, V_{CP} = 15 V, $T_j \geq 25$ °C	-23		-12	µA
		V_S = 7 V, V_{CP} = 15 V, $T_j < 25$ °C	-23		-10	µA

Table 5. Electrical characteristics (continued)

(7 V ≤ V_S ≤ 18.5 V; -40° C ≤ T_J ≤ 150 °C, unless otherwise specified.)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{CP}	Charge pump current	V_S = 12 V, V_{CP} = 20 V, $T_j \geq 25$ °C	-70		-45	µA
		V_S = 12 V, V_{CP} = 20 V, $T_j < 25$ °C	-70		-38	µA
t_{CP}	Charging time	$V_{CP} = V_S$ + 8 V C_{CP} = 100 pF			200	µs
$V_{SCP\ off}$	Overvoltage shut down		20		30	V
$V_{SCP\ hys}$	Overvoltage shut down hysteresis (1)		50	200	1000	mV
f_{CP}	Charge pump frequency (1)		100	250	400	KHz
Gate drivers						
I_{GSo}	Gate source current	$V_G = V_S$	-5	-3	-1	mA
I_{GSi}	Gate sink current	$V_G \geq 0.8$ V	1	3	5	mA
I_{GCP}	Charge pump current on the gate	V_S = 12 V, V_G = 20 V, $T_j \geq 25$ °C	-60		-35	µA
		V_S = 12V, V_G = 20 V, $T_j < 25$ °C	-60		-28	µA
Drain - source sensing						
V_{PR}	Bias current programming voltage	10 µA ≤ I_{PR} ≤ 100 µA; $V_D \geq 4$ V	1.8	2	2.2	V
$I_{D\ Leak}$	Drain pin leakage current	V_S = 0 V; V_D =14 V	0		5	A
I_D	Drain pin bias current	$V_S \geq V_D$ + 1 V; $V_D \geq 5$ V	0.9 I_{PR}		1.1 I_{PR}	
I_{Smax}	Source pin input current	$V_S \geq V_D$ + 1 V; $V_D \geq 7$ V	10		60	A
V_{HYST}	Comparator hysteresis			20		mV
Timer						
V_{THi}	Timer threshold high		4	4.4	4.8	V
V_{TLo}	Timer threshold low		0.3	0.4	0.5	V
I_T	Timer current	IN = 5 V; V_T = 2 V IN = 0 V; $V_S < V_D$; $V_D \geq 5$ V; V_T = 2 V	0.4 I_{PR} -0.6 I_{PR}		0.6 I_{PR} -0.4 I_{PR}	
Inputs						
V_{LOW}	Input enable low voltage		-0.3		1	V
V_{HIGH}	Input enable high voltage		3		7	V
V_{INhys}	Input enable hysteresis(1)		50	200	500	mV
I_{IN}	Input source current	$V_{IN} \leq 3$ V	-30		-5	µA
I_{EN}	Enable sink current	$V_{EN} \geq 1$ V	5		30	µA
t_d	Transfer time IN/ENABLE	V_S = 14 V $V_G = V_S$; Open Gate			2.5	µs

1. Not measured guaranteed by design.

Function is given for supply voltage down to 5.5V.
Function means: the channels are controlled from the inputs, some other parameters may exceed the limit. In this case the programming voltage and timer threshold will be lower. This leads to a lower protection threshold and time.

4 Functional description

The triple high-side Power-MOS Driver features all necessary control and protection functions to switch on three Power-MOS transistors operating as High-Side switches in automotive electronic control units. The key application field is relays replacement in systems where high current loads, usually motors with nominal currents of about 40 A connected to ground, has to be switched.

A high signal at the EN pin enables all three channels. With enable low gates are clamped to ground. In this condition the gate sink current is higher than the specified 3 mA. An enable low signal makes also a reset of the timer.

A low signal at the inputs switch on the gates of the external MOS. A short circuit at the input leads to permanent activation of the concerned channel. In this case the device can be disabled with the enable pin. The charge pump loading is not influenced due to the enable input.

An external N-channel MOS driver in high side configuration needs a gate driving voltage higher than V_S. It is generated by means of a charge pump with integrated charge transfer capacitors and one external charge storage capacitor C_{CP}.

The charge pump is dimensioned to load a capacitor CCP of 33 nF in less than 20 ms up to 8V above V_S. The value of C_{CP} depends on the input capacitance of the external MOS and the decay of the charge pump voltage down to that value where no significant influence on the application occurs.

The necessary charging time for C_{CP} has to be respected in the sequence of the input control signals.

As a consequence the lower gate to source voltage can cause a higher drop across the Power-MOS and get into overload condition. In this case the overload protection timer will start.

After the protection time the concerned channel will be switched off. Channel 3 is not equipped with an overload protection. The same situation can occur due to a discharge of the storage capacitor caused by the gate short to ground. The gate driver that is supplied from the pin CP, which is the charge pump output, has a sink and source current capability of 3 mA. For a short-circuit of the load (source to ground) the L9380 has no gate to source limitation. The gate source protection must be done externally.

Channel 1 and 2 provide drain to source voltage sensing possibility with programmable shut-off delay when the activation threshold was exceeded.

This threshold V_{DSmin} is set by the external resistor R_D. The bias current flowing through this resistor is determined by the programming resistor R_{PR}. This external resistor R_{PR} defines also the charge and discharge current of the timer capacitor C_{CT}. The drain to source threshold V_{DSmin} and the timer shut off delay time T_{off} can be calculated:

$$V_{DSmin} = V_{PR}\left(\frac{R_D}{R_{PR}}\right)$$

$$T_{off} = 4.4\ C_T\ R_{PR}$$

In application which don't use the overload protection or if one channel is not used, the Timer pin of this channel must be connected to ground and the drain pin with a resistor to V_{bat}.

The timing characteristic illustrates the function and the meaning of V_{DSmin} and T_{off} (see *Figure 6*). The input current of the overload sense comparator is specified as I_{Smax}. The sum $I_{PR} + I_{Dmax}$ generates a drop across the external resistor R_D if the drain pin voltage is higher than the source pin (see *Figure 4*). In the switching point the comparator input source pin currents are equal and the half of the specified current I_{Smax}. For an offset compensation equal external resistors (RD = RS) at drain and source pin are imperative. The drain sense comparator, which detects the overload, has a symmetrical hysteresis of 20 mV (see *Figure 5*).

Exceeding the source pin voltage by 10 mV with respect to the drain voltage forces the timer capacitor to discharge. Decreasing the source pin voltage 10 mV lower than the drain pin voltage an overload of the external MOS is detected and the timer capacitor will be loaded. After reaching a voltage at pin CT higher than the timer threshold V_{Thi} the influenced channel is switched off. In this case the overload is stored in the timer capacitor.

The timer capacitor will be discharged with a 'High' signal at the input (see *Figure 3*). After reaching the lower timer threshold V_{TLo} the overload protection is reset and the channel is able to switch on again.

Figure 3. Timing characteristic

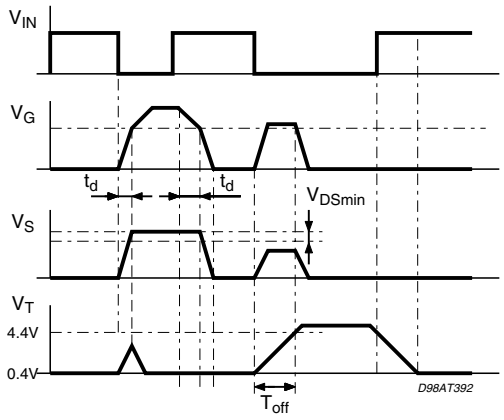


Figure 4. Drain, source input current.

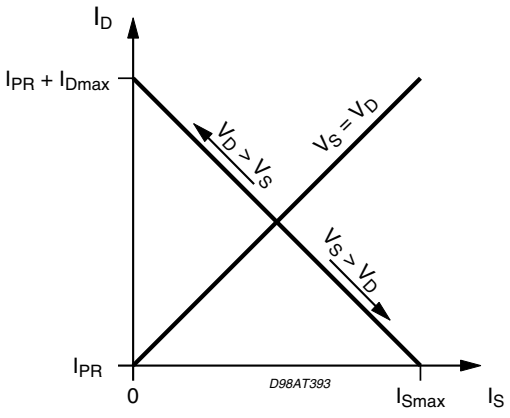
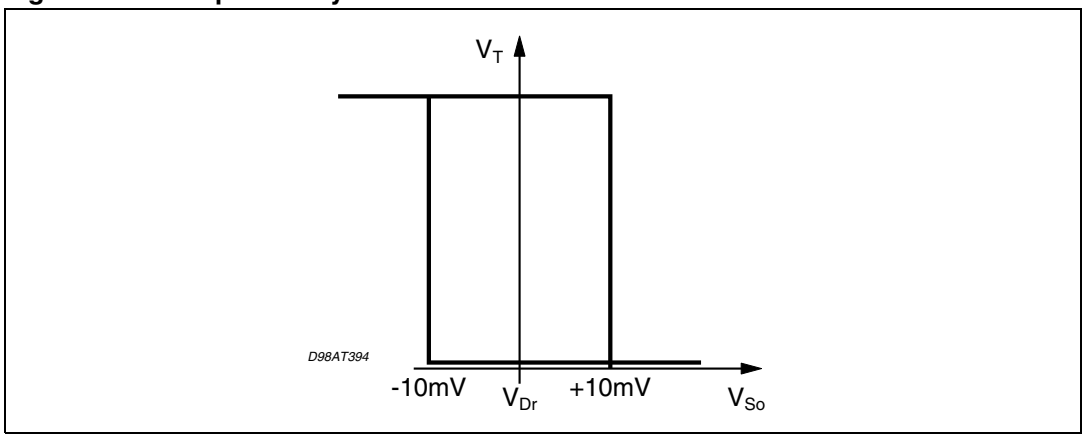


Figure 5. Comparator hysteresis



The application diagram is shown in *Figure 6*. Because of the transients present at the power lines during operation and possible disturbances in the system the external resistors are necessary.

Positive ISO-Pulses at Drain, Gate Source are clamped with an active clamping structure. The clamping voltage is less than 60V. Negative Pulses are only clamped with the ESD-Structure less than -15 V. This transients lower than -15 V can influence the other channels.

In order to protect the transistor against overload and gate breakdown protection diodes between gate and source and gate and drain has to be connected. In case of overvoltage into V_S (V_S > 20 V) the charge pump oscillation is stopped.

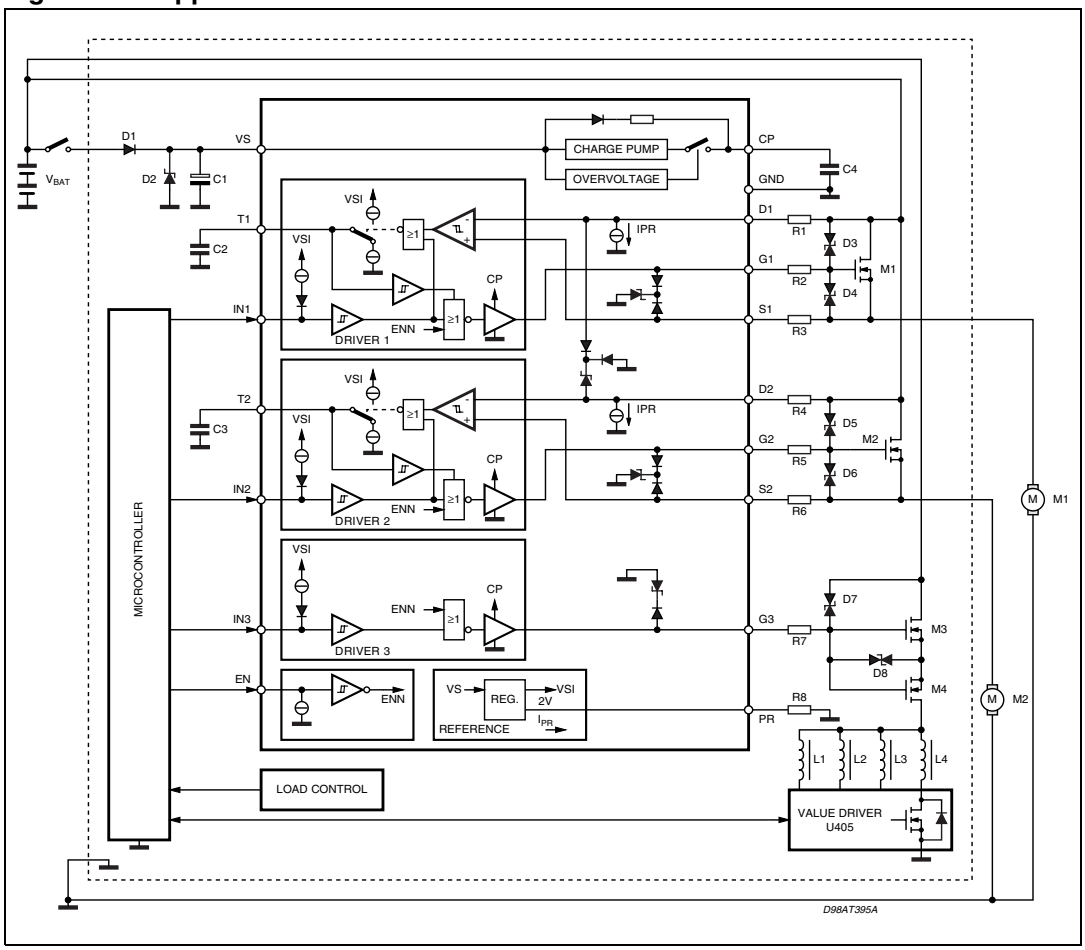
Then the charge pump capacitor will be loaded by a diode and a resistor in series up to V_S (see *Figure 1*). In this case the channels are not influenced. In reverse battery condition the pins D1, D2, S1, S2 follow the battery potential down to -13 V (high impedance) and the gate driver pins G1, G2 is referred to S1, S2. In this way it is assured that M1 and M2 will not be driven into the linear conductive mode. This protection function is operating for V_{S1}, V_{S2} down to -15 V. The gate driver output G3 is referred to the D1 in this case. This function guarantees that the source to source connected N-Channel MOS transistors M3 and M4 remains OFF.

All the supplies and the in- and output of the PC Board are supplied with a 40 wires flat cable (not used wires are left open). This cable is submitted to the RF in the strip-line like described in DIN 40839-4 or ISO 11456-5.

The measured circuit was build up on a PCB board with ground plane. In the frequency range from 1 MHz to 400 MHz and 80 % AM-modulation of 1 kHz with field strength of 200 V/m no influence to the basic function was detected on a typical device.

The failure criteria is an envelope of the output signal with 20 % in the amplitude and 2 % in the time.

Figure 6. Application circuit



Recommendations to the application circuit: The timer and the charge capacitors are loaded with an alternating current source. A short ground connection of the charge capacitor is indispensable to avoid electromagnetic emigrations. The dimension of the resistors RD, RG and RS have to respect the maximum current during transients at each pin.

4.1 Typical characteristics curve

Depending on production spread, certain deviations may occure. For limits see *Table 5*.

Figure 7. Charge loading time as function of V_S (V_{cp} = 8 V +V_S)

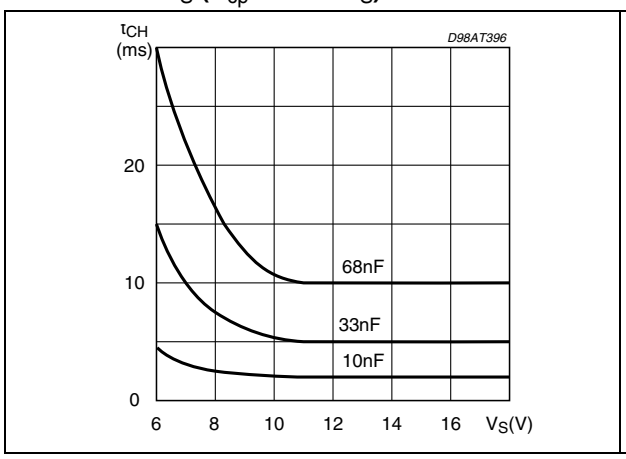


Figure 8. Charge pump current as function of the charge voltage

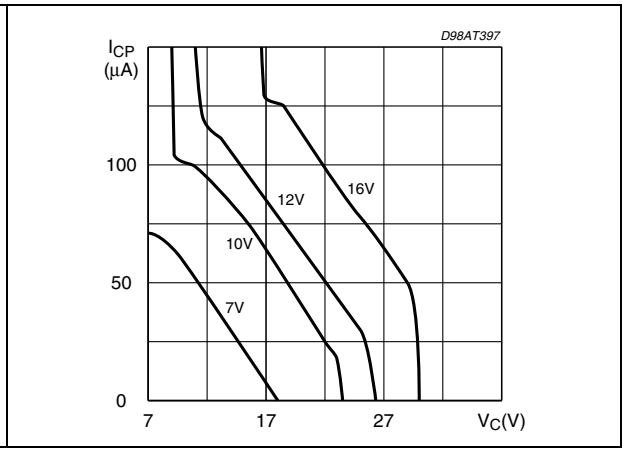


Figure 9. Ground loss protection gate discarge current for source voltage

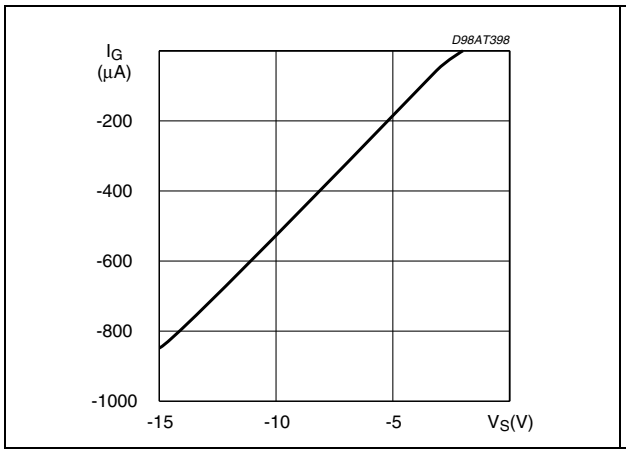


Figure 10. Input current as function of the input voltage

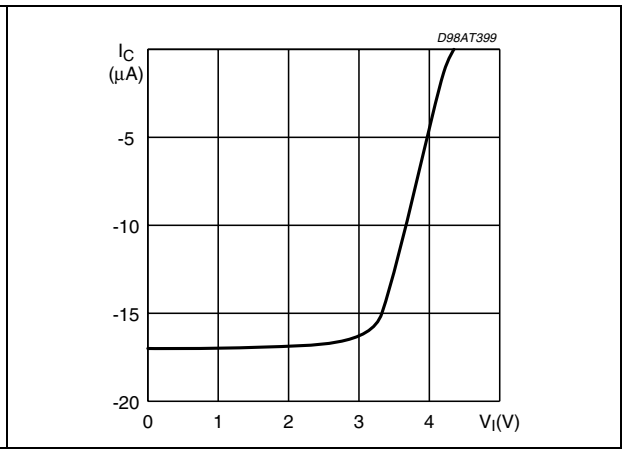


Figure 11. Overvoltage shutdown of the charge pump with hysteresis

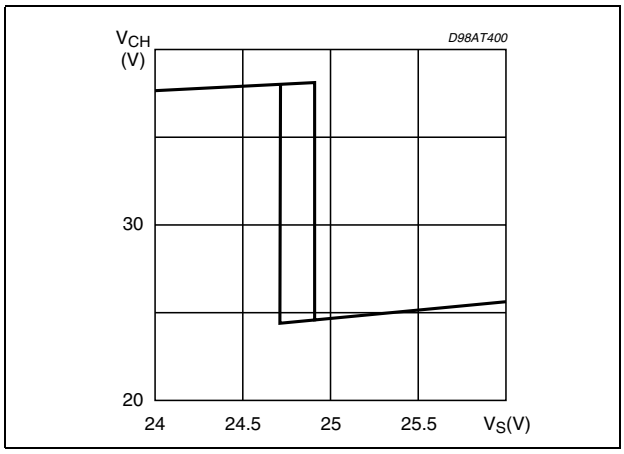


Figure 12. Measured circuit (The EMS of the device was verified in the below described setup)

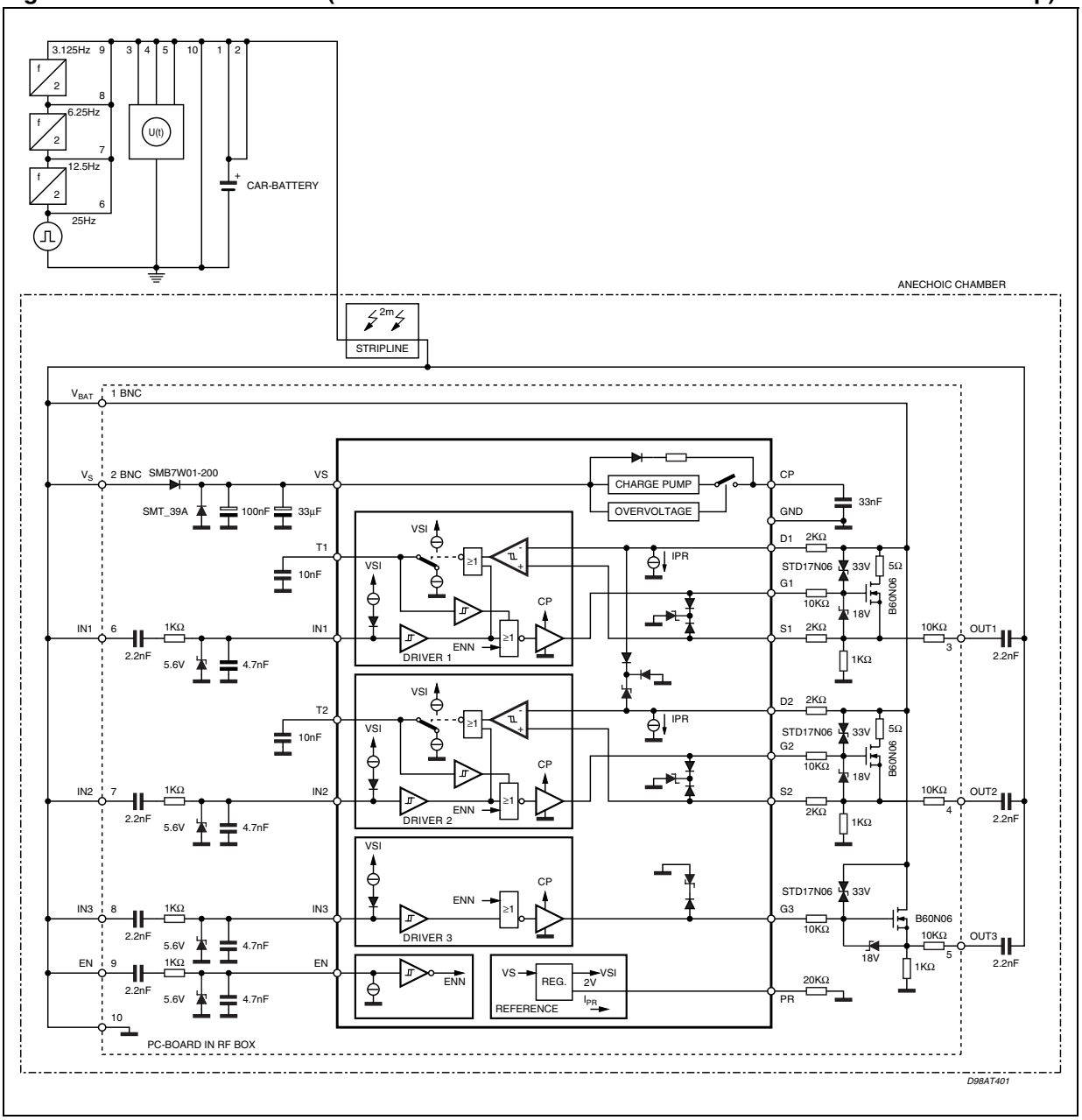
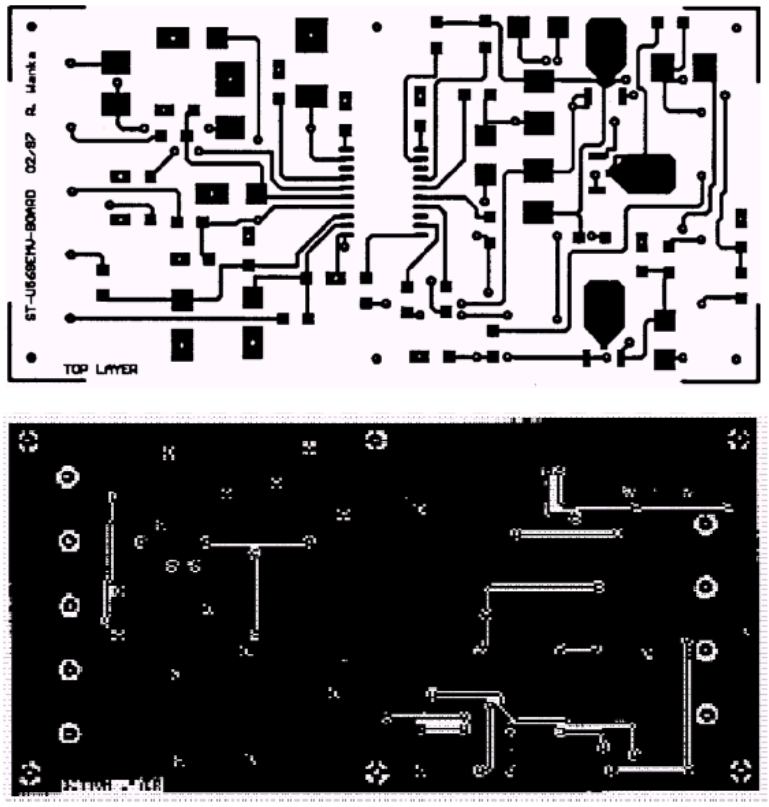


Figure 13. Printed circuit board (PCB)



4.1.1 Electromagnetic emission classification (EME)

Electromagnetic emission classes presented below are typical data found on bench test. For detailes test description please refer to "Electromagnetic Emission (EME) Measurement of Integrated Circuits, DC to 1 GHz" of VDE/ZVEI work group 767.13 and VDE/ZVEI work group 767.14 or IEC project number 47A 1967Ed. This data is targeted to board designers to allow an estimation of emission filtering effort required in application. All measurements are done with the EMS-board (See *Figure 12* and *13*).

Table 6. Electromagnetic emission classification

Pin	EME class			Remark
VCP	G	-	w	

Note: Electromagnetic Emission and Susceptivity is not tested in production.

5 Package information

In order to meet environmental requirements, ST (also) offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

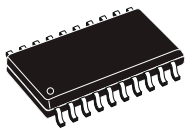
ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 14. SO20 mechanical data and package dimensions

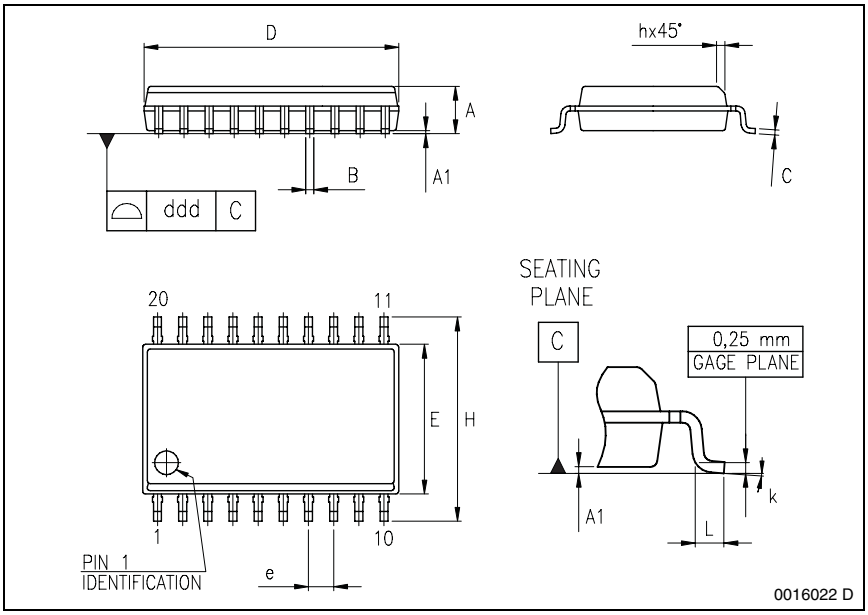
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.10		0.30	0.004		0.012
B	0.33		0.51	0.013		0.200
C	0.23		0.32	0.009		0.013
D (1)	12.60		13.00	0.496		0.512
E	7.40		7.60	0.291		0.299
e		1.27			0.050	
H	10.0		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA



SO20



6 Revision history

Table 7. Document revision history

Date	Revision	Changes
20-May-2003	1	Initial release.
05-Mar-2008	2	Document reformatted. Modified *Figure 6: Application circuit*.